WHAT IS CLAIMED IS:

1. A cache memory device comprising:

at least one cache memory storing copy data of a main memory, and

a bank control circuit, connected to said at least one cache memory, and capable of generating a plurality of control signals for access, said bank control circuit receiving a signal indicative of cache capacity and permitting at least one control signal selected out of said plurality of control signals to access said at least one cache memory, respectively, in accordance with said signal.

2. The cache memory device according to claim 1, wherein said bank control circuit controls access to said at least one cache memory in such a manner that one accessing operation implements access to only one out of said at least one cache memory.

3. The cache memory device according to claim 1, wherein said at least one cache memory has a plurality of cache memories, said cache memory device further comprising a power control circuit for controlling power supply to said plurality of cache memories connected to said bank control circuit based on said signal,

said power control circuit supplying a power to only one or more cache memories accessed with said at least one control signal selected by said bank control circuit out of said plurality of cache memories.

4. The cache memory device according to claim 1, wherein a cache address indicating an address of said main memory and including a tag and an index is input to said cache memory device,

a bit position occupied by said tag and said index is fixed in said cache address,

said at least one cache memory has a tag memory setting said index in said cache address to be an address, and

said tag memory stores said tag in said cache address,

said cache memory device further comprising:

a cache peripheral circuit for linking said index in said cache address input to said cache memory device when one or more cache memories accessed with said at least one control signal selected by said bank control circuit is accessed, to data in said tag memory stored in said address indicated by said index, and for generating and outputting a copy back address,

a copy back method using said copy back address being employed as a writing method for said main memory.

5. The cache memory device according to claim 1, wherein a cache address indicating an address of said main memory and including a tag and an index is input to said cache memory device,

a bit position occupied by said tag and said index is fixed in said cache address,

said at least one cache memory has a tag memory setting said index in said cache address to be an address, and

said tag memory stores said tag in said cache address,

said cache memory device further comprising:

a comparator for comparing said tag in said cache address input to said cache memory device when one or more cache memories accessed with said at least one control signal selected by said bank control circuit is accessed, to data in said tag memory stored in said address indicated by said index in said cache address, and for detecting their

coincidence/non-coincidence.

6. The cache memory device according to claim 1, wherein said at least one cache memory has a plurality of cache memories,

a cache address indicating an address of said main memory and including a tag is input to said cache memory device,

a bit position occupied by said tag is fixed in said cache address,

said plurality of cache memories have respective tag memories for storing said tag in said cache address, and

said respective tag memories store plural pieces of fixed data peculiar to said plurality of cache memories, respectively, each of said plural pieces of fixed data corresponding to a part of said tag.

7. The cache memory device according to claim 1, wherein said at least one cache memory has a plurality of cache memories, and

said plurality of cache memories have the same memory capacity.

8. A method of designing a cache memory device comprising at least one cache memory for storing copy data of a main memory, wherein said method comprises the steps of;

(a) designing a bank control circuit connectable to a first predetermined number of plural cache memories, and capable of permitting one or more cache memories of the first predetermined number of plural cache memories to be accessed, and changing the number of said one or more cache memories to be permitted to be accessed;

(b) designing a first cache memory device including said bank control circuit

designed in said step (a); and

(c) designing a second cache memory device including said bank control circuit designed in said step (a);

said step (b) including the step of:

(b–1) designing a second predetermined number of cache memories which is equal to or smaller than said first predetermined number, and

said step (c) including the step of:

(c–1) designing a third predetermined number of cache memories which is equal to or smaller than said first predetermined number and is different from said second predetermined number.

9. The method of designing a cache memory device according to claim 8, wherein said cache memory device receives a cache address indicating an address of said main memory and including a tag and an index,

wherein a bit position occupied by said tag and said index is fixed in said cache address,

said at least one cache memory has a tag memory setting said index in said cache address to be an address, and

said tag memory stores said tag in said cache address,

said method further comprising the step of:

(d) designing a cache peripheral circuit linking said index in said cache address received by said cache memory device when said at least one cache memory is accessed, to data in said tag memory stored in said address indicated by said index, and generates and outputs a copy back address, wherein

a copy back method using said copy back address is employed as a writing

method for said main memory, and

said first and second cache memory devices further comprising said cache peripheral circuit designed in said step (d) are designed at said steps (b) and (c), respectively.

10. The method of designing a cache memory device according to claim 8, wherein said cache memory device receives a cache address indicating an address of said main memory and including a tag and an index,

a bit position occupied by said tag and said index is fixed in said cache address,

said at least one cache memory has a tag memory setting said index in said cache address to be an address,

said tag memory stores said tag in said cache address,

said method comprising the step of:

(e) designing a comparator comparing said tag in said cache address received by said cache memory device when said at least one cache memory is accessed, to data in said tag memory stored in said address indicated by said index in said cache address, and detects their coincidence/non-coincidence, wherein

said first and second cache memory devices further comprising said comparator designed in said step (e) are designed at said steps (b) and (c), respectively.

11. A method of designing a cache memory device comprising at least one cache memory for storing copy data of a main memory;

said method comprising the steps of:

(a) designing a first cache memory device; and

(b) designing a second cache memory device after said step (a),

said step (a) including the step of:

(a-1) designing a bank control circuit connectable to a first predetermined number of plural cache memories, and capable of permitting one or more cache memories of the first predetermined number of plural cache memories to be accessed and changing the number of said one or more cache memories to be permitting to be accessed, and

said step (b) including the steps of:

(b–1) designing a second predetermined number of cache memories; and

(b–2) redesigning said bank control circuit designed in said step (a) in such a manner that said second predetermined number of cache memories are connected when said second predetermined number is greater than said first predetermined number.

12. The method of designing a cache memory device according to claim 11, further comprising the step of:

(c) describing design data about said bank control circuit by using a hardware descriptive language which employs, as a parameter, a memory capacity corresponding to a total number of the first predetermined number of plural cache memories, prior to said step (b),

at said step (b–2), a memory capacity corresponding to said second predetermined number being substituted for said parameter, thereby redesigning said bank control circuit designed in said step (a).

13. The method of designing a cache memory device according to claim 11, wherein said cache memory device receives a cache address indicating an address of said

main memory and including a tag and an index,

a bit position occupied by said tag and said index is fixed in said cache address,

said at least one cache memory has a tag memory setting said index in said cache address to be an address, and

said tag memory stores said tag in said cache address,

said method of designing further comprising the step of:

(d) designing a cache peripheral circuit linking said index in said cache address received by said cache memory device when said at least one cache memory is accessed, to data in said tag memory stored in said address indicated by said index, and generating and outputting a copy back address, wherein

a copy back method using said copy back address is employed as a writing method for said main memory,

at said step (a), said first cache memory device includes said cache peripheral circuit designed at step (d), and

at said step (b), said second cache memory device further comprising said cache peripheral circuit designed in said step (d) is designed.

14. The method of designing a cache memory device according to claim 11, wherein said cache memory device receives a cache address indicating an address of said main memory and including a tag and an index,

a bit position occupied by said tag and said index is fixed in said cache address,

said at least one cache memory has a tag memory setting said index in said cache address to be an address, and

said tag memory stores said tag in said cache address,

said method of designing further comprising the step of:

(e) designing a comparator comparing said tag in said cache address received by said cache memory device when said at least one cache memory is accessed, to data in said tag memory stored in an address indicated by said index in said cache address, and detecting their coincidence/non-coincidence, wherein

at said step (b), said second cache memory device further comprising said comparator designed in said step (e) is designed.

15. A bank control circuit controlling an access to a cache memory, comprising;

a decoder receiving first and second signals and outputting bank select signals such that one of the bank select signals is active in accordance with said first and second signals, wherein said first signal is indicative of a cache capacity used in the cache memory and said second signal is a part of an address supplied to the cache memory, and

signal output circuits provided correspondingly to the bank select signals, respectively, each signal output circuit receiving a control signal for accessing the cache memory and a corresponding bank select signal, and permitting the control signal to be output to the cache memory in response to an active state of said corresponding bank control signal while inhibiting said control signal to be output to the cache memory in response to a non-active state of said corresponding bank control signal.